REMARKS

Claims 1-22 are all the claims currently pending in this Application.

Claim Amendments

With this Amendment, Applicants amend claims 10 and 17. These amendments are fully-supported in the originally-filed specification. Applicants respectfully request entry of these amendments.

Prior Art Rejections

Claims 1-22 are rejected under 35 U.S.C. § 102(e) as allegedly unpatentable over Zhang (U.S. Patent 7,120,856). Applicants respectfully traverse this rejection.

Applicants submit that Zhang fails to disclose a parity-checkmatrix that consists of sub-matrices of a Kronecker product of two permutation matrices[1]. Regarding this limitation, the

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[1] Claim 1 recites: "a Low-Density Parity-Check code, whose parity-checkmatrix consists of a Kronecker product of two permutation matrices,...a plurality of address generation means for generating an address of said memory means on the basis of the first permutation matrix of said sub-matrix of a Kronecker product; and a plurality of shuffle network means for determining a connection between said variable node function means on the basis of the second permutation matrix in said sub-matrix of a Kronecker product";

Claim 10 recites: " a Low-Density Parity-Check Code, whose parity-checkmatrix consists of sub-matrices of a Kronecker product of a first permutation matrix and a second permutation matrix, ... address generation means for generating addresses of a plurality of memory means that store a received value and a message generated during said decoding, on a basis of the first permutation matrix of said sub-matrix of a Kronecker product; and shuffle network means for determining a connection between variable node function means and check node function means on a basis of the second permutation matrix in said sub-matrix of a Kronecker product, which is a permutation changed in a same cycle as that of said address generation means."

Claim 17 recites: "a Low-Density Parity-Check Code, whose parity-checkmatrix consists of sub-matrices of a Kronecker product of a first permutation matrix and a second permutation matrix, ... generating an address of a memory storing a received value and a message generated during said decoding on a basis of the first permutation matrix of said sub-matrix of a Kronecker product; and

...(footnote continued)

Examiner refers to columns 5 and 6 of Zhang. These columns discuss the creation of a parity check matrix H as shown in Figure 2, which consists of submatrices H_1 and H_2. However, H_1 and H_2 are not formed by a Kronecker product of permutation matrices. Rather, each of H_1 and H_2 is a number of LxL "identity" matrices, each of which is obtained by a cyclic shift of an LxL matrix. "Step 100" indicates that H_1 and H_2 are constructed so that $H=[H_1^T, H_2^T]^T$ defines a (2,k)-regular LDPC code denoted as C_2. However, this also, does not disclose that the parity check matrix H, consisting of H_1 and H_2 is the Kronecker product of two permutation matrices.

Therefore, Applicants submit that Zhang fails to disclose that a "parity-checkmatrix consists of sub-matrices of a Kronecker product of two permutation matrices" and similarly fails to disclose "a plurality of shuffle network means for determining a connection between said variable node function means *on the basis of the second permutation matrix in said sub-matrix of a Kronecker product*".

Additionally, Applicants submit that a global shuffle network among the plurality of CNU and VNU and memory units, as shown in Figures 3 and 4 of Zhang corresponds to a local shuffle network among the SN(1)-SN(k) in Figure 1 of the present Application.

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connecting a plurality of variable node functions in said decoding and a plurality of check node functions in said decoding on a basis of the second permutation matrix of said sub-matrix of a Kronecker product, which is a permutation changed in a same cycle as that of an address generation means".

Since identical $P_{i,k}$ are used in a small block in the present invention, address generation circuits AG(j), as shown in Figure 1 of the present invention, can be common for D memories in a small block[2]. On the other hand, Zhang requires an address generation circuit for each memory.

Applicants also note that Zhang relates to (3,k)-regular LDPC cord, as can be understood by the discussion of assigning parameters, as in claim 1 of Zhang. On the other hand, the present invention relates to a configuration of a decoding device having a configuration which is a Kronecker product of permutation matrices which is not limited to (3,k)-regular.

Therefore, in view of at least the above, Applicants submit that claims 1, 10, and 17 are patentable over Zhang and that claims 2-9, 11-16, and 18-22 are patentable at least by virtue of their dependencies. Applicants respectfully request that the rejection of claims 1-22 over Zhang be reconsidered and withdrawn.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

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[2] Claim 10 recites: "address generation means *for generating addresses of a plurality of memory means*".

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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Date: November 26, 2007